We claim:

1. A method of fetching processor instructions, the method comprising:

receiving a request for an instruction;

searching a cache system at a first level for the instruction; and

searching the cache system at a second level for the instruction in parallel with the first level based on a prediction of whether the instruction will be found at the first level.

2. The method of claim 1 further including:

determining a parameter value corresponding to a first level search history for the instruction;

comparing the parameter value to a predetermined threshold; and

initializing the search of the cache system at the second level when the parameter value exceeds the predetermined threshold.

3. The method of claim 2 further including determining a cache miss value corresponding to the first level search history.

4. The method of claim 3 further including tracking a number of cache misses for a predetermined number of cache searches corresponding to the instruction.

5. The method of claim 4 further including initializing the search of the cache system at the second level when the number cache misses for the predetermined number of cache searches is greater than zero.

6. The method of claim 2 further including storing the parameter value to a computer readable storage medium.

Sub A2

7. The method of claim 6 further including storing the parameter value in the cache system.

8. The method of claim 2 further including retrieving the parameter value from a computer readable storage medium.

9. The method of claim 8 further including retrieving the parameter value from the cache system.

10. The method of claim 1 further including receiving a front end re-start instruction.

11. The method of claim 1 further including searching the cache system at a trace cache level for the instruction, the trace cache level being the first level of the cache system.

12. The method of claim 1 further including searching an instruction cache for the instruction, the instruction cache being the second level of the cache system.

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13. The method of claim 1 further including searching the cache system at a main memory level for the instruction, the main memory level being the second level of the cache system.

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14. A method of searching a cache system at a second level, the method comprising:

determining a parameter value corresponding to a first level search history for an instruction;

comparing the parameter value to a predetermined threshold; and

initializing a search of the cache system at the second level when the parameter value exceeds the predetermined threshold.

15. The method of claim 14 further including determining a cache miss value corresponding to the first level search history.

16. The method of claim 15 further including tracking a number of cache misses for a predetermined number of cache searches corresponding to the instruction.

17. The method of claim 15 further including initializing the search of the cache system at the second level when the number cache misses for the predetermined number of cache searches is greater than zero.

18. The method of claim 15 further including storing the parameter value to a computer readable storage medium.

19. The method of claim 15 further including retrieving the parameter value from a computer readable storage medium.

20. A method of fetching processor instructions, the method comprising:

determining a parameter value corresponding to a trace cache level search history for a front end re-start instruction;

storing the parameter value to a computer readable storage medium;

receiving a request for the instruction;

retrieving the parameter value from the computer readable storage medium;

comparing the parameter value to a predetermined threshold;

initializing a search of the cache system at a second level when the parameter value exceeds the predetermined threshold;

searching a cache system at a trace cache level for the instruction; and

querying a decoder for the instruction in parallel with the trace cache level based on a prediction of whether the instruction will be found at the first level;

said prediction being based on the parameter value and the predetermined threshold.

21. The method of claim 20 further including determining a cache miss value corresponding to the trace cache level search history.

22. The method of claim 21 further including tracking a number of cache misses for a predetermined number of cache searches corresponding to the instruction.

23. The method of claim 22 further including initializing the querying of the decoder when the number cache misses for the predetermined number of cache searches is greater than zero.

24. A computer readable storage medium storing a set of instructions capable of being executed by a processor to:

receive a request for an instruction;

search a cache system at a first level for the instruction; and

search the cache system at a second level for the instruction in parallel with the first level based on a prediction of whether the instruction will be found at the first level.

25. The storage medium of claim 24 wherein the set of instructions are further capable of being executed by the processor to:

determine a parameter value corresponding to a first level search history for the instruction;

compare the parameter value to a predetermined threshold; and

initiate the search of the cache system at the second level when the parameter value exceeds the predetermined threshold.

26. A processor instruction management system comprising:

an instruction supply engine having a cache system, the supply engine to generate a decoded instruction based on a request for the decoded instruction; and

an execution core to execute the decoded instruction, the instruction supply engine searching the cache system at a first level for the instruction and searching the cache system at a second level in parallel with the first level based on a prediction of whether the instruction will be found at the first level.

27. The instruction management system of claim 26 wherein the instruction supply engine further includes:

a shift register to receive a first level search history signal for the instruction, the signal defining a number of cache misses for a predetermined number of cache searches corresponding to the instruction; and

an OR gate coupled to the shift register, the OR gate generating a miss prediction signal when the number of cache misses for the predetermined number of cache searches is greater than zero.

28. The instruction management system of claim 27 wherein the shift register has three data outputs, the predetermined number of cache searches being three.